FPGA based

Implementation of wireless sensor networks
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Abstract

The Wireless sensor Network provides 24/7 online temperature monitoring of critical connection points in electrical equipment. Continuous monitoring provides the means to evaluate the equipment’s current condition and detect abnormalities at an early stage. Utilizing wireless technology eliminates the need for special cables and provides lower installation costs than other types of online condition monitoring equipment.
Block Diagram

System board:

Sensor Network 1

- Zigbee Module
- RS232 UART
- 12-BIT SPI
- Temperature Sensor LM35

Sensor Network 2

- Zigbee Module
- RS232 UART
- 12-BIT SPI
- Temperature Sensor LM35

Control unit:

- Zigbee Module
- Temperature Network 1
  Network 2

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**Explanation:**

Temperature data is transmitted from the sensors to a nearby receiver via Zigbee Modem. The receiver is connected to a computer via serial Communication.

**Importance:**

Conduction problems caused by loose connections or deterioration of contact surfaces result in a local temperature rise, which contributes to the reduction of the contact quality. Thermal runaways induced by conduction problems deteriorate the insulating material and cause disruptive dielectric discharges resulting in arcing faults. The ability to continuously monitor the condition of energized equipment (online monitoring) provides operation and maintenance personnel with a means to:

1) Determine the operational status of equipment

2) Evaluate present condition of equipment

3) Detect abnormal conditions in a timely manner

4) Initiate actions to prevent possible forced outages
The consequences of such faults are serious enough to justify the efforts to install a temperature monitoring system to help prevent electric equipment from disaster.

**Relevance of the proposal:**

The proposed system is an embedded system which will closely monitor temperature at the machineries and to eliminate the difficulties involved in the system by reducing human intervention to the best possible extent.

The system comprises of

- Zigbee
- Analog to Digital Converter
- FPGA

When any of the above mentioned climatic parameters cross a safety threshold which has to be maintained to protect the crops, the sensors sense the change and the fpga reads this from the data at its input ports after being converted to a digital form by the ADC. The fpga then performs the needed actions by employing relays until the strayed-out parameter has been
brought back to its optimum level. Since a fpga is used as the heart of the system, it makes the set-up low-cost and effective nevertheless.

**Benefits:**

Provides continuous online monitoring of critical connection points

- Monitors multiple points simultaneously
- Detects abnormal conditions in a timely manner
  - Early warning alarms help prevent costly downtime
  - Initiate actions to prevent future failure
- Extends maintenance intervals
- Easy and low-cost installation for wireless sensors

**This project is divided into three phases:**

1. Identifying the appropriate sensor for measuring temperature. Temperature sensor to be used is LM35 so that low cost aim can be successful with best stability.

2. Design of controller using FPGA, sensor interface

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3. Choosing wireless Communication Module

4. Development of a user interface software.

**Tool required:**

Software: Xilinx ISE 10.1i or above

Language: VHDL

Hardware: 1. Spartan3an FPGA kit

2. Zigbee Module

3. JTAG Cable

4. PC (Monitoring Purpose)
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity adc_ch0 is
port ( clk   : in std_logic;
       led    : out std_logic_vector(7 downto 0);
       cs    : out std_logic;
       sc  : out std_logic;
       do    : out std_logic;
       dout    : out std_logic;
       din   : in std_logic);
end adc_ch0;

architecture Behavioral of adc_ch0 is

type state is (spi,conversion,transmission);

signal presentstate : state := spi;
signal f : std_logic;


type arr is array (0 to 12) of std_logic_vector(9 downto 0);
signal store : arr;
begin

process(clk)
variable i,j,k : integer := 0;
variable tot : std_logic_vector(11 downto 0) := "000000000000";
begin

if clk'event and clk = '1' then
if presentstate = spi then
    if i <= 50 then
        i := i + 1;
        sc <= '1';
    elsif i > 50 and i < 100 then
        i := i + 1;
        sc <= '0';
    elsif i = 100 then
        i := 0;
        if j < 18 then
            j := j + 1;
        elsif j = 18 then
            j := 0;
        end if;
    end if;
end if;
end if;
end process;
presentstate <= conversion;

j := 0;
end if;
end if;

if j = 0 or j >= 18 then
    cs <= '1';
else
    cs <= '0';
end if;

if i > 40 and i < 60 then
    case j is
        when 0 => do <= '0';
        when 1 => do <= '1';
        when 2 => do <= '1';
        when 3 => do <= '1';
        when 4 => do <= '1';
        when others => null;
    end case;
end if;

if i >= 0 and i < 10 then
    case j is
when 6 => tot(11) := din;
when 7 => tot(10) := din;
when 8 => tot(9) := din;
when 9 => tot(8) := din;
when 10 => tot(7) := din;
when 11 => tot(6) := din;
when 12 => tot(5) := din;
when 13 => tot(4) := din;
when 14 => tot(3) := din;
when 15 => tot(2) := din;
when 16 => tot(1) := din;
when 17 => tot(0) := din;
when others => null;
end case;
end if;
end if;
-----------------------------------------------------------
---
if presentstate = conversion then
  cs <= '1';
  led(0) <= tot(9);
  led(1) <= tot(8);
  led(2) <= tot(7);
  led(3) <= tot(6);

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```plaintext
led(4) <= tot(5);
led(5) <= tot(4);
led(6) <= tot(3);
led(7) <= tot(2);

store(0) <= "1010101000"; -- T
store(1) <= "1010010100"; -- E
store(2) <= "1010001010"; -- M
store(3) <= "1001000000"; -- SPACE

if tot(9 downto 2) >= "00000000" and tot(9 downto 2) <= "00010100" then
    store(4) <= "1010011000";
    store(5) <= "1010011110";
elseif tot(9 downto 2) > "00010100" and tot(9 downto 2) <= "00010111" then
    store(4) <= "1001100010";
    store(5) <= "1001101000";
elsif tot(9 downto 2) > "00010111" and tot(9 downto 2) <= "00011010" then
    store(4) <= "1001100010";
```

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store(5) <= "1001110000";

elsif tot(9 downto 2) > "00011010" and tot(9 downto 2) <= "00011010" then
    store(4) <= "1001100100";
    store(5) <= "1001100000";

elsif tot(9 downto 2) > "00011101" and tot(9 downto 2) <= "00100000" then
    store(4) <= "1001100100";
    store(5) <= "1001100100";

elsif tot(9 downto 2) > "00100000" and tot(9 downto 2) <= "00100011" then
    store(4) <= "1001100100";
    store(5) <= "1001101000";

elsif tot(9 downto 2) > "00100011" and tot(9 downto 2) <= "00100110" then
    store(4) <= "1001100100";
    store(5) <= "1001101100";

elsif tot(9 downto 2) > "00100110" and tot(9 downto 2) <= "00101010" then

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store(4) <= "1001100100";
store(5) <= "1001110000";
-- 28
elsif tot(9 downto 2) > "00101010" and tot(9 downto 2) <= "00101110" then
store(4) <= "1001100110";
store(5) <= "1001100000";
-- 30
elsif tot(9 downto 2) > "00101110" and tot(9 downto 2) <= "00110010" then
store(4) <= "1001100110";
store(5) <= "1001100100";
-- 32
elsif tot(9 downto 2) > "00110010" and tot(9 downto 2) <= "00110101" then
store(4) <= "1001100110";
store(5) <= "1001101000";
-- 34
elsif tot(9 downto 2) > "00110101" and tot(9 downto 2) <= "00111000" then
store(4) <= "1001100110";
store(5) <= "1001101100";
-- 36
elsif tot(9 downto 2) > "00111000" and tot(9 downto 2) <= "00111011" then
store(4) <= "1001100110";
store(5) <= "1001110000";
elsif tot(9 downto 2) > "00111011" and tot(9 downto 2) <= "00111110" then
store(4) <= "1001101000";
store(5) <= "1001100000";
elsif tot(9 downto 2) > "00111110" and tot(9 downto 2) <= "01000001" then
store(4) <= "1001101000";
store(5) <= "1001101000";
elsif tot(9 downto 2) > "01000001" and tot(9 downto 2) <= "01000100" then
store(4) <= "1001101000";
store(5) <= "1001101000";
elsif tot(9 downto 2) > "01000100" and tot(9 downto 2) <= "01000111" then
store(4) <= "1001101000";
store(5) <= "1001101100";  -- 46
elsif tot(9 downto 2) > "01010000" and tot(9 downto 2) <= "01010101" then
store(4) <= "1001101000";
store(5) <= "1001110000";  -- 48
elsif tot(9 downto 2) > "01010101" and tot(9 downto 2) <= "11111111" then
store(4) <= "1010010000";
store(5) <= "1010010010";  -- 50
end if;
end if;

if i < 50000 then
    i := i + 1;
elsif i = 50000 then
    i := 0;
    presentstate <= transmission;
end if;

end if;

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if presentstate = transmission then
    cs <= '1';
    if i < 5209 then
        i := i + 1;
        dout <= store(k)(j);
    elsif i = 5209 then
        if j < 9 then
            j := j + 1;
        elsif j = 9 then
            j := 0;
            if k < 6 then
                k := k + 1;
            elsif k = 6 then
                presentstate <= spi;
                k := 0;
            end if;
        end if;
        i := 0;
    end if;
end if;
end if;
end process;
end Behavioral;
Conclusion

Wireless communication with FPGA using Zigbee using the serial port communication is an advantageous project; through this project you can control hardware from PC. People can control their electrical devices via PC. We think this product have high potential for marketing in the future.
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